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Density of States-Based Design of Metal Oxide Thin-Film Transistors for High Mobility and Superior Photostability

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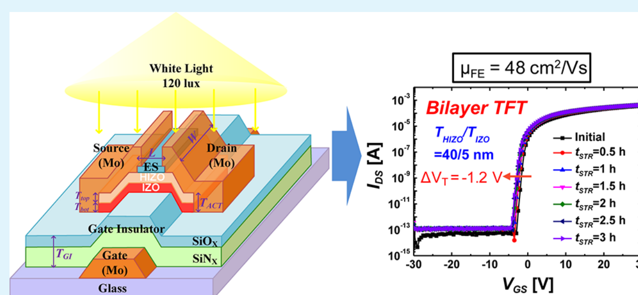
Supporting Information

ABSTRACT: A novel method to design metal oxide thin-film transistor (TFT) devices with high performance and high photostability for next-generation flat-panel displays is reported. Here, we developed bilayer metal oxide TFTs, where the front channel consists of indium-zinc-oxide (IZO) and the back channel material on top of it is hafnium-indium-zinc-oxide (HIZO). Density-of-states (DOS)-based modeling and device simulation were performed in order to determine the optimum thickness ratio within the IZO/HIZO stack that results in the best balance between device performance and stability. As a result, respective values of 5 and 40 nm for the IZO and HIZO layers were determined. The TFT devices that were fabricated accordingly exhibited mobility values up to 48 $cm^2/(V\ s)$, which is much elevated compared to pure HIZO TFTs (~13 $cm^2/(V\ s)$) but comparable to pure IZO TFTs (~59 $cm^2/(V\ s)$). Also, the stability of the bilayer device (−1.18 V) was significantly enhanced compared to the pure IZO device (−9.08 V). Our methodology based on the subgap DOS model and simulation provides an effective way to enhance the device stability while retaining a relatively high mobility, which makes the corresponding devices suitable for ultradefinition, large-area, and high-frame-rate display applications.



KEYWORDS: *metal oxide thin-film transistors, hafnium-indium-zinc-oxide, indium-zinc-oxide, photostability, density-of-states*

INTRODUCTION

High mobility ZnO-based metal oxide thin-film transistors (TFTs) have recently emerged as excellent substitutes for amorphous Si and/or polycrystalline Si TFTs, for next generation active matrix-liquid crystal display (AM-LCD) and active matrix-organic light emitting diode (AM-OLED) technology. Many AM display prototypes driven by amorphous indium-gallium-zinc-oxide (a-IGZO) TFTs have been demonstrated during the past few years.[1−9] However, recent reports show that the instability of TFT devices under negative bias thermal illumination stress (NBTIS) is a challenging issue that needs to be overcome in order to realize mass production of ZnO-based TFTs.[10,11] Therefore, the achievement of good stability under NBTIS while maintaining high mobility (e. g., higher than the field-effect mobility of a-IGZO TFTs typically in the range of 10−20 $cm^2/(V\ s)$) is crucial for the implementation of metal oxide TFTs in innovative applications such as 3-D, transparent, flexible, and lightweight systems.

One of the promising semiconductor materials is amorphous hafnium-indium-zinc-oxide (a-HIZO).[12−14] It is reported that the Hf ions may play a key role in improving the stability of the TFTs, due to their high oxygen bonding ability, hence suppressing the formation of oxygen vacancies.[12] However, increasing the Hf composition results in considerable loss in mobility and carrier concentration.[13] In our previous work, we were able to overcome this detriment by adopting bilayer active structures, where the Hf-content was modulated in each layer. The resulting device parameters were μ_{FE} (field-effect mobility) = 15 $cm^2/(V\ s)$, ΔV_T (NBTIS-induced threshold voltage shift) = −2.55 V, and SS (subthreshold swing) = 0.6−0.9 V/dec.[15]

In this Article, in order to further improve the device performance so that μ_{FE} values exceed 20 $cm^2/(V\ s)$, we report on bilayer metal oxide TFTs that consist of a combination of a-HIZO and amorphous indium-zinc-oxide (a-IZO) as separate active layers. A-IZO and a-HIZO were chosen as the promising combination for bilayer active structures, because the former is a well-known metal oxide with high mobility[16,17] and the latter has a good stability although the mobility is relatively low.[12−14] High performance devices were obtained, with electrical parameters such as μ_{FE} = 48 $cm^2/(V\ s)$, SS = 0.28 V/dec,

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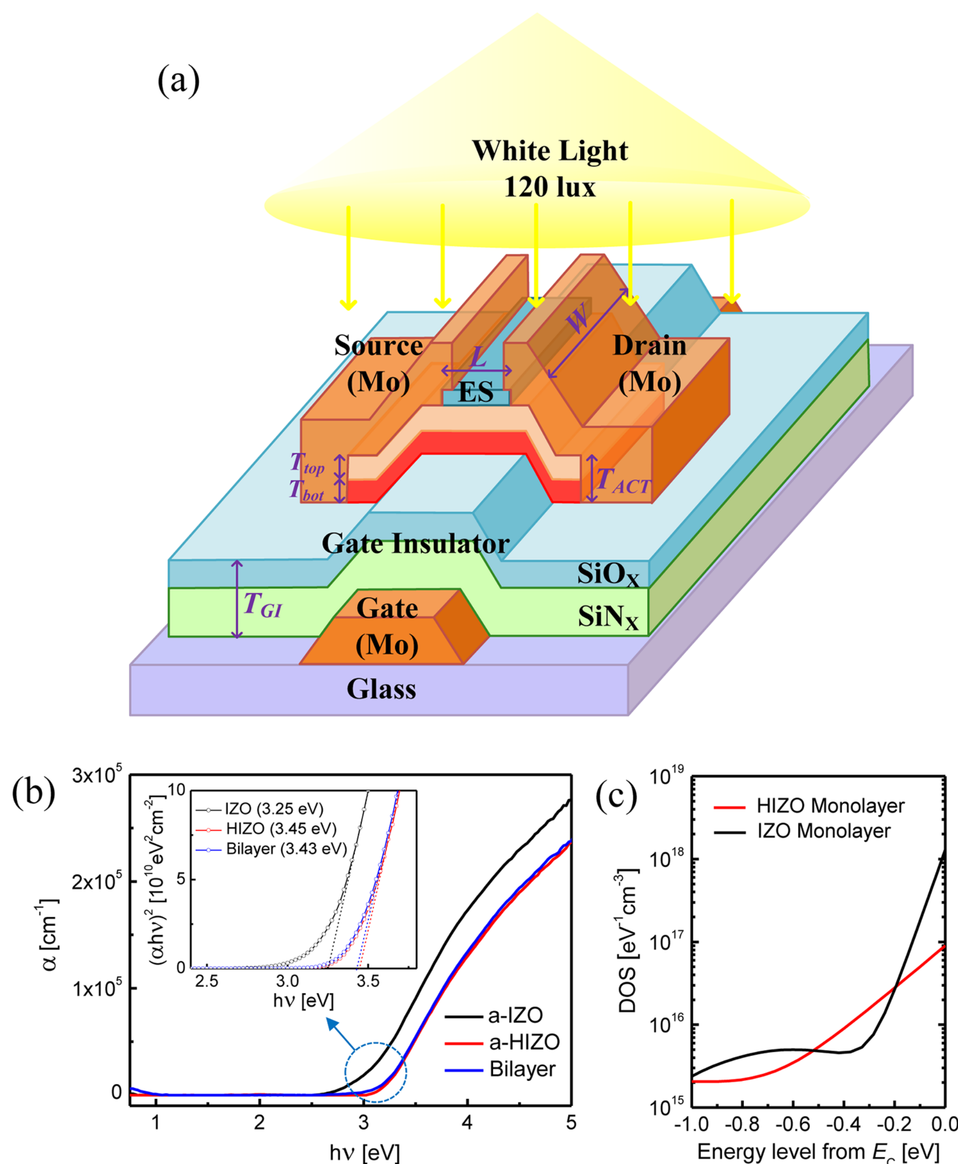

Figure 1. (a) Schematic illustration of the fabricated TFT structure. (b) Optical absorption coefficient measured by spectroscopic ellipsometry. Insets show the Tauc plot; $(\alpha h\nu)^2$ as a function of photon energy hν, where ν is the photon frequency, indicating the optical bandgap (E_g) for IZO monolayer (3.25 eV), HIZO monolayer (3.45 eV), and HIZO/IZO bilayer (3.43 eV). (c) Acceptor-like DOS distribution [$g_A(E)$] of IZO and HIZO monolayers, which was extracted by the frequency dependence of $C-V$ characteristics.[21]

and $\Delta V_T = -1.18$ V, which are critical for the fabrication of high resolution, fast frame rate displays. The above performance was achieved through a systematic study on the trade-off between mobility and stability, by applying subgap density-of-states (DOS) analyses. This work provides a quantitative analysis that correlates the material properties to the resulting device characteristics, especially by studying the DOS parameters extracted from electrical measurements.

EXPERIMENTAL SECTION

Device Fabrication. All samples were prepared on glass substrates. Prior to device fabrication, the substrates were chemically cleaned using aqueous mixtures of H_2SO_4–H_2O_2, followed by deionized water rinsing. Bottom-gate and top-contact TFTs were fabricated using a standard semiconductor fabrication process. The integration of metal oxide bilayer-TFTs was done by sputter depositing a 200-nm-thick Mo gate at room temperature and subsequently growing a dielectric stack of a 350-nm-thick SiN_x and a 50-nm-thick SiO_x at 350 °C by the plasma-enhanced chemical vapor deposition (PECVD). Three different types of active layer configurations were employed. The first one consists of an a-IZO monolayer, and the second one is a monolayer of a-HIZO, each with nominal thickness T_{ACT} = 40 nm. The last type is a bilayer active stack, where the active layer consists of a thin a-IZO (T_{bot} = 5 nm grown directly on the gate insulator) and a top a-HIZO film (T_{top} = 40 nm) as schematically shown in Figure 1a. The individual active layers were deposited at room temperature by radio frequency (RF) magnetron cosputtering using separate targets of In_2O_3, ZnO, and HfO_2. The RF power supplied to each of the aforementioned targets was adjusted so as to control the composition of the IZO and HIZO films being deposited. The compositions of the films were analyzed by inductively coupled plasma atomic emission spectrometry. The cation ratio (atomic %) was Hf/In/Zn = 10:35:55 for the HIZO monolayer and In/Zn = 85:15 for the IZO monolayer. Subsequently, a 100-nm-thick SiO_x etch stopper layer was deposited at 200 °C by PECVD, and then, 200-nm-thick Mo was sputtered at room temperature to form the source-drain electrodes. Finally, a 200-nm-thick PECVD SiO_x film was deposited at 350 °C as the passivation layer. All patterning was done by photolithography and appropriate use of wet or dry etching. The above transistors were then annealed in

Table 1. Measured Device Parameters

parameter	HIZO monolayer TFT	IZO monolayer TFT	HIZO/IZO bilayer TFT
V_{ON} [V] @ I_{DS} = 1 pA	0.87 ± 0.04	−7.9 ± 0.40	−1.86 ± 0.09
V_T [V] constant current method @ I_{DS} = 1 nA	1.6 ± 0.08	−7.18 ± 0.40	−1.02 ± 0.05
V_T [V] linear extrapolation	5.0 ± 0.25	−4.85 ± 0.24	2.15 ± 0.11
I_{ON} [A] @ V_{GS} = 30 V	9.94 ± 0.50 (×10^{-7})	6.03 ± 0.30 (×10^{-6})	3.87 ± 0.19 (×10^{-6})
I_{OFF} [A] @ V_{GS} = −20 V	1.5 ± 0.08 (×10^{-13})	1.46 ± 0.07 (×10^{-13})	1.24 ± 0.06 (×10^{-13})
I_{ON}/I_{OFF}	6.63 ± 0.33 (×10^{6})	4.13 ± 0.21 (×10^{7})	3.12 ± 0.16 (×10^{7})
SS [V/dec]	0.2 ± 0.01	0.27 ± 0.01	0.28 ± 0.01
linear μ_{FE} [cm^2/V·s] @ V_{DS} = 0.1 V	13.72 ± 0.69	59.13 ± 2.96	48.28 ± 2.41
saturation μ_{FE} [cm^2/V·s] @ V_{DS} = 10 V	5.11 ± 0.26	41.51 ± 2.08	43.24 ± 2.16

air for 1 h at 250 °C. Cross-sectional TEM was utilized to investigate the film uniformity and thickness (Hitachi 7600 operating at 300 kV). The channel length, channel width, and gate-to-S/D overlap length were 20, 50, and 10 μm, respectively.

Electrical Characterization and Measurement Conditions. All electrical properties were measured using a Keithley 4200-SCS semiconductor parameter analyzer, and the threshold voltage (V_T), subthreshold swing (SS) and the field-effect mobility (μ_{FE}) were extracted in compliance with the gradual channel approximation. The V_T was defined as the gate voltage that induces a drain current of 1 nA. For the NBTIS experiments, a V_{GS} of −20 V was applied, and a V_{DS} of 10 V was maintained at a substrate temperature of 60 °C for each device. A halogen lamp with a luminance of 120 lux was used in order to supply visible light. During the stress experiment, transfer curves were collected every 30 min for a total duration of 3 h.

Device Simulation. The SILVACO ATLAS-2D device simulator was used for all device simulation. The DOS parameters in Table S1 (Supporting Information) were used in the device simulation and made it possible to estimate the effect of bilayer thickness on the electrical characteristics. The simulated results were then compared with the experimental data.

RESULTS AND DISCUSSION

A schematic device structure is depicted in Figure 1a with an inverted staggered bottom-gate configuration. The fabrication details can be found in the Experimental Section. Three different active layer configurations were employed for the fabrication of TFTs. The first consists of a single a-IZO layer, and the second one is a single a-HIZO layer with nominal thickness T_{ACT} (the thickness of active layer) = 40 nm. The last device has a bilayer active structure, where the active layer consists of a-IZO (T_{bot} = 5 nm directly in contact with the gate insulator) and a-HIZO (T_{top} = 40 nm on top of the a-IZO layer) as shown in Figure 1a. The geometrical parameters of the fabricated TFTs are as follows: T_{GI} (gate insulator thickness) = 350/50 nm (SiN_x/SiO_x) = 275 nm (equivalent oxide thickness), W (channel width) = 50 μm, L (channel length) = 20 μm, and L_{ov} (gate-to-S/D overlap length) = 10 μm, respectively. The T_{ACT} of HIZO or IZO monolayer TFT was 40 nm as mentioned above, and the finally optimized T_{top}/T_{bot} (= 40/5 nm) of HIZO/IZO bilayer TFT was determined by device simulation, which will be discussed later in this Article.

The material properties of HIZO and IZO monolayers were first examined. From grazing incidence angle X-ray diffraction (XRD) patterns of the HIZO and IZO thin films (with a thickness of 40 nm) deposited on Si substrates, no sharp peak other than the Si substrate signal is observed, which indicates the presence of an amorphous-like structure for both HIZO and IZO films (see Figure S1, Supporting Information). A cross-sectional transmission electron microscope (TEM) image of the fabricated HIZO/IZO bilayer TFT indicates that the gate, insulator, channel, etch stopper, source/drain, and passivation layers are well-defined with excellent thickness uniformity (see Figure S1, Supporting Information). Further high-resolution TEM and selected area diffraction pattern (SADP) studies confirm the formation of an amorphous phase in the HIZO/IZO bilayer. A high angle annular dark field scanning transmission electron microscope (HAADF-STEM) image clearly distinguishes the IZO and HIZO layers with uniform thickness, suggesting the absence of interdiffusion (see Figure S1, Supporting Information). X-ray photoelectron spectroscopy (XPS) measurements were performed to analyze the O 1s, Zn 2p, and In 3d core levels of the HIZO and IZO films (see Figure S2, Supporting Information). The XPS O 1s spectra could be deconvoluted into two peaks, one located at ~529.5 eV and the other at ~530.8 eV. Prior studies of IZO indicate that the peak at ~530 eV corresponds to lattice oxygen in a fully coordinated environment, while the peak at higher binding energies near 531 eV arise from oxygen-deficient environments, most likely to be related to oxygen vacancies.[18] Note that the relative area (15.1%) of the latter in IZO is larger than that (11.8%) in HIZO. The oxygen vacancy-related peaks could be more clearly observed in the Zn 2p and In 3d peaks (see Figure S2, Supporting Information). Noticeably, the oxygen vacancy-related peaks located at higher binding energies in HIZO are negligible (0.9−1.8%) compared with those (17.2−17.7%) in IZO. Such difference may be attributed to the strong oxygen−hafnium ionic bonds that form in HIZO.[12] Therefore, the carrier electron density of the IZO monolayer TFT is expected to be much higher than that of the HIZO monolayer TFT, because oxygen vacancies are in general known to be sources of free electrons.[19,20] The relative indium cation compositions of the IZO and HIZO films determined by inductively coupled plasma-atomic emission spectroscopy (ICP-AES) are 85% and 35%, respectively. The carrier mobility of the IZO monolayer TFT is thus expected to be much higher than that of the HIZO device, as the conduction band minimum (CBM) mainly consists of In 5s orbitals and the wave functions corresponding to energy levels located near the CBM become more delocalized with an increase in In content.

Next, in order to relate the analyzed material properties with electrical parameters that allow device simulation, the modeling of subgap density-of-states (DOS) was conducted. The distribution of subgap DOS is a very important physical and process-dependent parameter that strongly influences the bias/photo instability as well as the electrical performance. Figure 1b shows the optical absorption coefficients (α) as a function of photon energy (hν) for the IZO monolayer, HIZO monolayer, and HIZO/IZO bilayer, which were measured using spectroscopic ellipsometry; the optical bandgaps (E_g) obtained based on the Tauc plot (inset of Figure 1b) for the IZO monolayer, HIZO monolayer, and HIZO/IZO bilayer are 3.25, 3.45, and

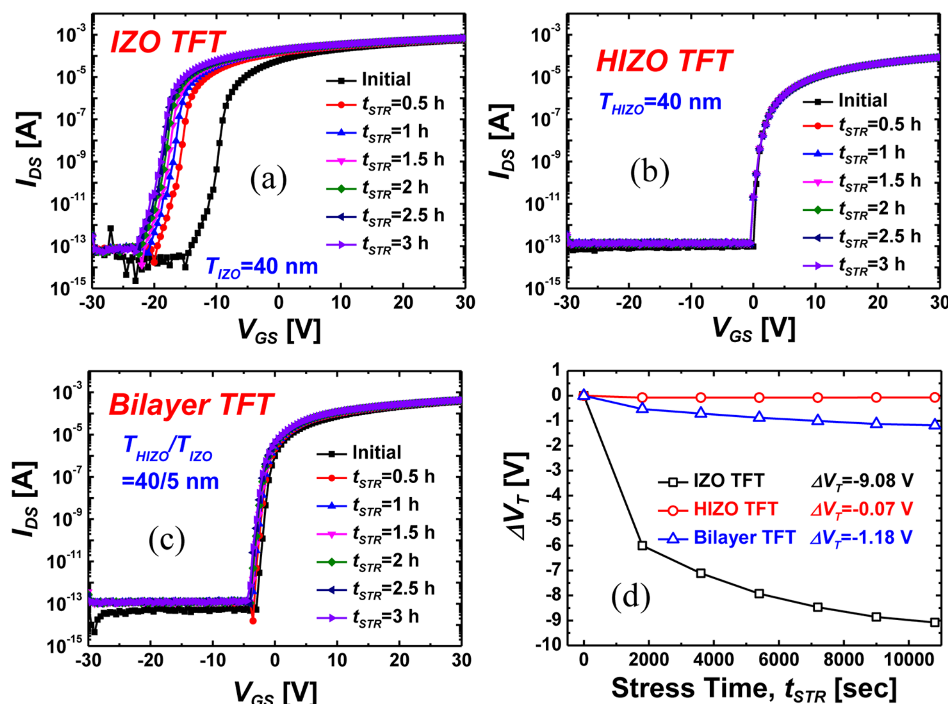

Figure 2. The measured NBTIS time (t_{NBTIS}) evolutions of transfer characteristics of (a) the IZO monolayer, (b) the HIZO monolayer, and (c) the HIZO/IZO bilayer TFTs. (d) The threshold voltage shift (ΔV_T) as a function of the t_{NBTIS} for the three kinds of TFTs.

3.43 eV, respectively. For the IZO monolayer, a larger absorption is found near the CBM, which is corroborated by the larger Urbach tail (subgap states) near the band edge in comparison with the a-HIZO monolayer. This suggests that more subgap states near CBM exist in IZO rather than HIZO, which is also confirmed by the following DOS characterization. The acceptor-like DOS distribution [$g_A(E)$] was then extracted using the frequency dependence of $C-V$ characteristics of the IZO monolayer and the HIZO monolayer TFTs,[21] as seen in Figure 1c. This method is based on the assumption that the measured $C-V$ characteristics are frequency dependent due to not only the transit time of carriers but also the frequency-dispersion of capture/emission process into/out of subgap states. More details are given in Supporting Information S4. Consistently, with the optical absorption data (Figure 1b), the $g_A(E)$ near CBM is higher in IZO compared to HIZO, which also explains why the SS of HIZO TFTs is smaller than that of IZO TFTs (see Table 1). This is because a larger amount of subgap states near CBM raises the Fermi-energy level to the conduction band edge more slowly with respect to the gate bias.

We electrically measured the output and transfer characteristics in the linear/saturation regimes (see Figure S3, Supporting Information). The typical device parameters of two monolayer TFTs are summarized in the first two columns in Table 1. As expected, the μ_{FE} of IZO TFT is much higher than that of the HIZO TFT whereas the SS of the HIZO TFT is lower than that of IZO TFT. Therefore, our XPS, ICP-AES, and DOS model analyses are reasonable and consistent with one another.

The devices were then stressed under NBTIS with a negative gate bias (gate-to-source voltage (V_{GS}) = −20 V) and a drain-to-source voltage (V_{DS}) = 10 V, which is the current standard for evaluating device stability in industry, in the presence of visible light (white light with a luminance of 120 lux) at a substrate temperature of 60 °C. A large parallel negative shift (ΔV_T = −9.08 V) was observed in the IZO monolayer TFT after the NBTIS time (t_{NBTIS}) = 3 h (Figure 2a). This is due to the enhanced electron−hole pair generation from subgap states (larger Urbach tail; see Figure 1b) in IZO under illumination, which induces larger concentrations of photoinduced charge carriers that become trapped at the semiconductor/gate-insulator interface. As a result, transfer curves shift in the negative direction. In contrast, the HIZO TFT operates stably with no apparent performance degradation (ΔV_T = −0.07 V), as shown in Figure 2b. Here, the addition of hafnium is believed to suppress oxygen vacancy formation,[12] weakening the Urbach tail and thus reducing the density of subgap defect states. However, the advantages of HIZO TFTs including small SS and ΔV_T are compromised by the relatively low μ_{FE} (13.72 $cm^2/(V\ s)$) compared to that (59.13 $cm^2/(V\ s)$) of IZO TFTs, as summarized in Table 1.

In order to systematically design a bilayer metal oxide TFT that has comparable mobility and superior NBTIS stability with respect to the a-IZO device, DOS-based device simulation was done using the SILVACO Atlas-2D device simulator.[22] A-IZO was chosen as the bottom layer (with thickness T_{bot} above the gate insulator: as seen in Figure 1a) to utilize the superior mobility of IZO. The extracted E_g and subgap DOS were directly incorporated into the device simulation, as displayed in Figure 3a,b. The subgap DOSs of IZO and HIZO monolayer were modeled with specific parameters (see Table S1, Supporting Information).

The TFT performances and stabilities were systematically simulated (or modeled) and optimized as a function of the total thickness ($T_{top} + T_{bot}$) and the thickness ratios (T_{top}/T_{bot}) of HIZO/IZO bilayer TFTs, as seen in Figure 3c−g. Note that there are competing total thickness dependences in terms of performance and stability. In order to achieve higher I_{ON}, smaller SS, and lower vertical electric field (E_{ver}) near the gate

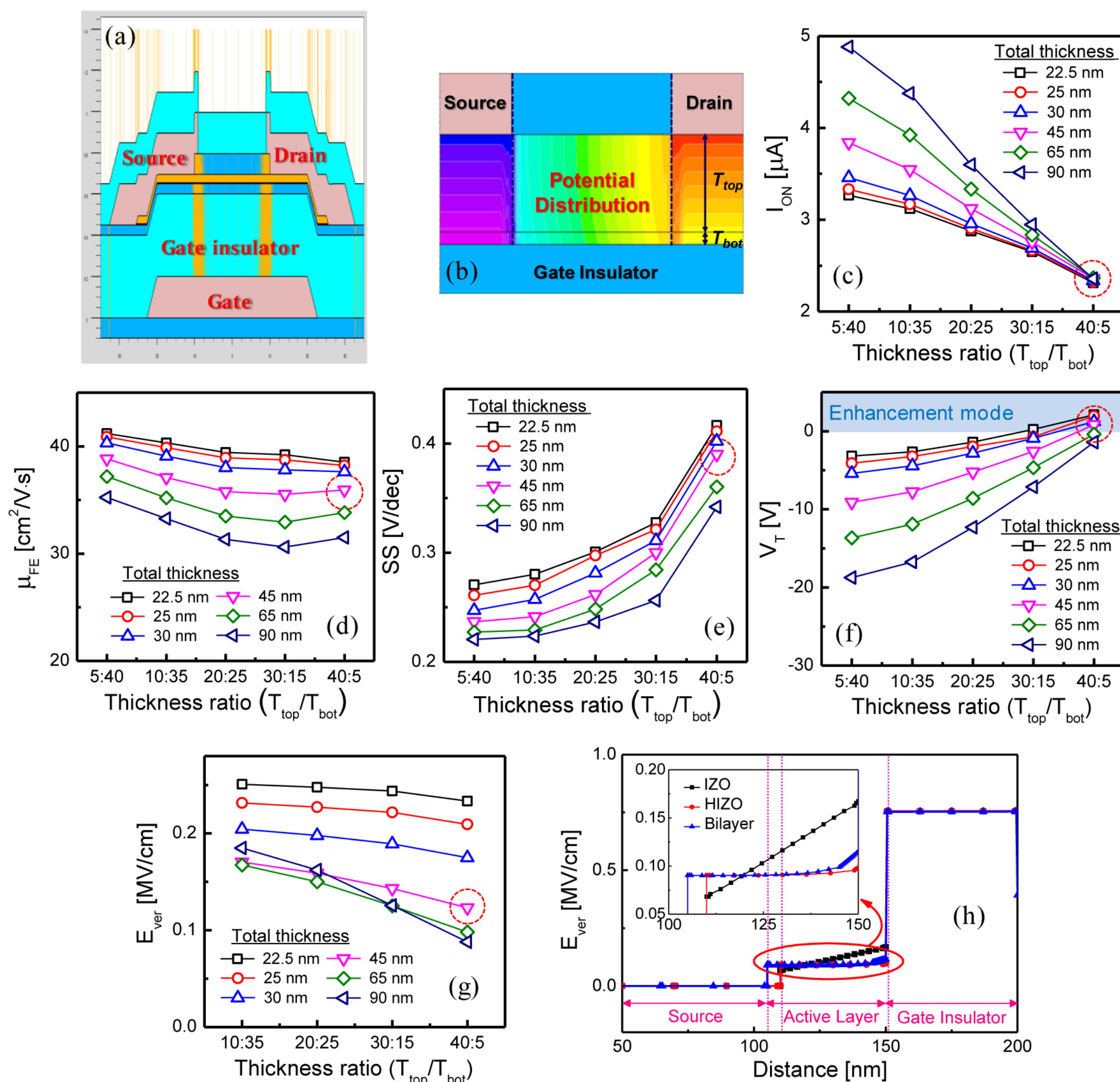

Figure 3. Schematic illustration of (a) the TFT structure used in the device simulation and (b) the potential contour. The simulated thickness ratio (T_{top}/T_{bot}) and total thickness (T_{top} + T_{bot}) dependence of (c) on current (I_{ON}), (d) linear field-effect mobility (μ_{FE}), (e) subthreshold swing (SS), (f) threshold voltage (V_T) extracted by linear extrapolation, and (g) vertical electric field (E_{ver}) at the interface with the gate insulator in HIZO/IZO bilayer TFTs. The selected optimum condition (T_{top}/T_{bot} = 40/5 nm) was marked by the red circle. (h) The simulated E_{ver} distributions over the vertical direction of IZO, HIZO monolayer (with T_{ACT} = 40 nm), and HIZO/IZO bilayer TFTs (with T_{top}/T_{bot} = 40/5 nm).

insulator to ensure lower carrier trap densities (in other words, better stability), a thicker bilayer stack is required. On the other hand, to obtain higher μ_{FE} and more positive V_T, a thinner stack is needed. For example, for the best stability, it is natural to choose the thickest bilayer stack (90 nm); however, this results in depletion mode operation (i.e., highly negative V_T) and the smallest μ_{FE} values among the tested structures (22.5−90 nm). Therefore, it is reasonable to select an intermediate thickness of 45 nm, which provides reasonably high mobility, high stability, and positive V_T among the simulated architectures. For the thickness ratio (T_{top}/T_{bot}) of HIZO/IZO bilayer TFT, we note that the IZO thickness should be minimized to operate the TFT in enhancement mode (V_T > 0 V). Our careful study on the IZO deposition by sputtering revealed that a thickness of at least 5 nm is required to have a uniform film over the entire substrate without the formation of separate island-like morphology. Finally, the case of T_{top}/T_{bot} = 40/5 nm is considered as the optimum condition with respect to performance as well as NBTIS stability. Indeed, as shown in Figure 3h, compared with the IZO monolayer TFT, it is noteworthy that the E_{ver} of HIZO/IZO bilayer TFT near the gate insulator is reduced to a level similar to that in the HIZO monolayer TFT, which suggests the NBTIS stability of the HIZO/IZO bilayer TFT (T_{top}/T_{bot} = 40/5 nm) can be improved to a level comparable to that of the HIZO monolayer TFT.

As a result, T_{top}/T_{bot} = 40/5 nm was used to fabricate the actual bilayer devices. The *I*−*V* characteristics of HIZO/IZO bilayer TFTs with T_{top}/T_{bot} = 40/5 nm were measured (see Figure S3, Supporting Information), and their device parameters are summarized in the last column of Table 1. The device simulation results for HIZO/IZO bilayer as well as IZO or HIZO monolayer TFTs reproduce the measured transfer characteristics very well, which verifies our DOS model is reasonable and the used DOS-based TFT simulation framework is quantitatively well calibrated. As expected from our simulations, the I_{ON} and μ_{FE} of the HIZO/IZO bilayer TFT are much higher than those of the HIZO monolayer TFT,

while they are slightly lower than those of the IZO monolayer TFT.

Next, we investigated the stability of HIZO/IZO bilayer TFTs under NBTIS. Figure 2c shows the parallel negative shifts in the transfer characteristics of the HIZO/IZO bilayer TFT, in which $\Delta V_T = -1.18$ V was observed after $t_{NBTIS} = 3$ h. The t_{NBTIS} evolutions of threshold voltage V_T are summarized in Figure 2d. It should be noted that the HIZO/IZO bilayer TFT exhibits $\mu_{FE} = 48$ cm^2/(V s), SS = 0.28 V/dec, and $\Delta V_T = -1.18$ V after $t_{NBTIS} = 3$ h under illumination. These excellent properties provide a great potential for applications in AM-LCD and AM-OLED backplanes with large-area integration, high resolution, and high-frame rate.

■ CONCLUSION

In summary, we developed a novel device structure for ultra high-performance and highly stable TFT by adopting a HIZO (stability booster)/IZO (mobility booster) bilayer channel. It was found that the systematic and quantitative optimization of the total thickness ($T_{top} + T_{bot}$) and its thickness components (T_{top}/T_{bot}) in combination with a sophisticated DOS-based design of HIZO and IZO played a critical role in achieving high performance and high stability. The methodology based on the subgap DOS model and simulation was demonstrated to be an effective tool to design metal oxide TFTs with high mobility and superior photostability for applications in next-generation flat-panel displays.

■ ASSOCIATED CONTENT

Supporting Information

Associated content, including (i) XRD patterns and TEM images, (ii) XPS spectra, (iii) I−V data, and (iv) extracted DOS parameter. This material is available free of charge via the Internet at http://pubs.acs.org.

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Author Contributions

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Notes

The authors declare no competing financial interest.

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